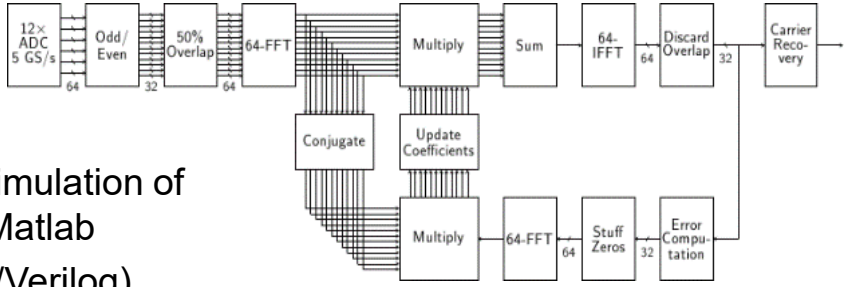
HiWi Openings:

Optical Coherent Receiver DSP Implementation

Karlsruhe Institute of Technology

At home or on the move - ubiquitous use of network connected devices result in significant traffic growth which has to be transported over metro, long-haul, and inter-datacenter networks. This demands high-capacity, spectrally efficient, and cost effective electro-optic transceivers for reliable communication. Digital signal processing (DSP) along with high speed digital-to-analog converters (ADC) and polarization-diverse coherent receivers allows to mitigate various transmission impairments (i.e., chromatic dispersion, polarization-mode dispersion, and laser phase noise, etc.)

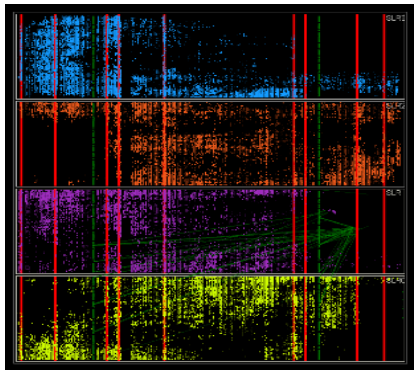


Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
FF	1302984	2443200	53.33
LUT	875685	1221600	71.68
Memory LUT	121975	344800	35.38
I/O	1075	1200	89.58
BRAM	82	1292	6.35
DSP48	1780	2160	82.41
BUFG	10	128	7.81
MMCM	2	24	8.33
GT	2	20	10.00

Your Tasks:

- High-level logic design and simulation of coherent DSP algorithms in Matlab
- Logic implementation (VHDL/Verilog)
- Design verification using Questa/Modelsim
- Hardware implementation using Xilinx Vivado



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